REMARKS

The present application was filed on November 21, 2003 with claims 1 through 20. Claims 1 through 20 are presently pending in the above-identified patent application. Claims 1, 4, 8, 11, and 14 are proposed to be amended herein.

Applicants note that an Information Disclosure Statement dated May 16, 2006 was submitted which discloses references cited in a European Search Report including United States Publication Number 2001/0026175 (hereinafter Ueno).

Independent Claims 1 and 8

Independent claims 1 and 8 are rejected under 35 U.S.C. §102(e) as being anticipated by Luo. In particular, the Examiner asserts that Luo discloses a sample and hold circuit. Among other features, the Examiner asserts that Luo also discloses (i) at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output (citing element C1 in FIG. 1); (ii) at least one output switch for selectively connecting said at least one capacitive element to said output (citing element S3 of FIG. 1); and (iii) an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage (FIG. 1: element 11; col. 3, lines 50-64).

Applicants note that, regarding element C1, Luo teaches that,

> continuing to refer to FIG. 1 and FIG. 2, **during quarter period 2** switch S1 connecting the first transconductor 10 to the operational amplifier 11 is open, and switch S2 connecting the sample and hold capacitor C2 to the output of the operational amplifier 11 is closed allowing capacitor C2 to be charged up to a voltage equal to that on capacitor C1. **Switches S4a and S4b remain closed.** Switch S6 is closed to discharge the voltage on the parasitic capacitance at the output of the transconductor 10. **All other switches are open during quarter period 2.**
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> Continuing to refer to FIG. 1 and FIG. 2, **during quarter period 3** switch S0 is closed to discharge the voltage on the feed back capacitor C1. Switch S5a is closed to connect input voltage $k_2$ $V_R$ to the input of the transconductor 10 and **switch S5b is closed to connect a voltage reference -$V_R$ to the (+) input terminal of the current summing operational amplifier 11**. Switch S6 remains closed to discharge the voltage on the parasitic capacitance at the output of the transconductor 10. **All other switches are open during quarter period 3.**
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> Continuing to refer to FIG. 1 and FIG. 2, during quarter periods 4 and 5 switches S1, S5a and S5b are closed, and all other switches are open. The

> feedback capacitor C1 is charged for one half clock period by the output of the transconductor 10 from the reference voltage $-V_R$ to a voltage $-V_y$. During quarter period 6 switches S5a and S5b remain closed and S3 is closed allowing a voltage equal to that on capacitor C1 to be put onto capacitor C3. Switch S6 is closed to discharge the capacitance on the parasitic capacitance at the output of the transconductor 10, and all other switches are open.
> (Col. 4, lines 23-53; emphasis added.)

Luo teaches that *switch S4b is closed and switch S5b is open during quarter 2*, and that *switch S4b is open and switch S5b is closed during quarter 3*. Thus, Luo actually *teaches away* from the present invention by teaching to ***not** limit* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*. Independent claim 1 requires an amplifier connected to said node, *wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage*. Independent claim 8 requires *limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element.*

In addition, independent claims 1, 8, and 14 have been amended to require limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a voltage that is more negative than an input signal of said NMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said NMOS switch to an output of said amplifier in a hold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switch by coupling said parasitic drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said PMOS switch to an output of said amplifier in a hold mode. Support for this amendment can be found in FIG. 6 and the associated text. Neither Luo nor Ueno disclose or suggest limiting leakage current in parasitic drain and source diodes using this technique.

Thus, Luo and Ueno, alone or in combination, do not disclose or suggest limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a voltage that is more negative than an input signal of said NMOS switch in a sample mode and by coupling said parasitic drain and

source diodes of said NMOS switch to an output of said amplifier in a hold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switch by coupling said parasitic drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said PMOS switch to an output of said amplifier in a hold mode, as required by independent claims 1, 8, and 14, as amended.

Additional Cited References

Beauducel was also cited by the Examiner for its disclosure of a resistor placed in parallel as disclosed in the sample and hold circuit of FIG. 4 ($R_1$). Although Beauducel is directed to a sample and hold circuit, Beauducel does *not* disclose or suggest the feature of limiting leakage current in parasitic drain and source diodes using this technique.

Thus, Beauducel et al. do not disclose or suggest limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a voltage that is more negative than an input signal of said NMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said NMOS switch to an output of said amplifier in a hold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switch by coupling said parasitic drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said PMOS switch to an output of said amplifier in a hold mode, as required by independent claims 1, 8, and 14, as amended.

Mills was also cited by the Examiner for its disclosure of a sample and hold circuit in which its hold time is 200 microseconds. Applicants note that Mills is directed to an analog to digital signal converter that includes an integrator and a sample and hold circuit. Mills does *not*, however, disclose or suggest the feature of limiting leakage current in parasitic drain and source diodes using this technique.

Thus, Mills et al. do not disclose or suggest limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a voltage that is more negative than an input signal of said NMOS

switch in a sample mode and by coupling said parasitic drain and source diodes of said NMOS switch to an output of said amplifier in a hold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switeh by coupling said parasitie drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and souree diodes of said PMOS switch to an output of said amplifier in a hold mode, as required by independent claims 1, 8, and 14, as amended.

Sandusky was also cited by the Examiner for its disclosure of a sample and hold circuit for a preamplifier in a disk drive. Applicants note that Sandusky is directed to a circuit for input switching for a read channel. Sandusky does *not*, however, disclose or suggest the feature of limiting leakage current in parasitic drain and source diodes using this technique.

Thus, Sandusky et al. do not disclose or suggest limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a voltage that is more negative than an input signal of said NMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said NMOS switch to an output of said amplifier in a hold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switch by coupling said parasitic drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said PMOS switch to an output of said amplifier in a hold mode, as required by independent claims 1, 8, and 14, as amended.

Conclusion

The rejections of the cited claims under sections 102 and 103 in view of Luo, Beauducel et al., Mills et al., Ueno, and Sandusky et al., alone or in combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner to this matter is appreciated.

Respectfully,

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